AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being configured to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being configured to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

a[[n]] selector circuit connected to said first and second receiver and driver pairs, said selector circuit selectively operating said first and second receiver and driver pairs according to a selection signal such that in a first operating mode said first receiver and driver pair passes data between said first bus segment and an I/O device[[,]] and bypasses said second bus segment, and in a second operating mode said first and second receiver and driver pairs pass data between respective adjacent bus segments and bypass said I/O device.

Claim 2 (original): An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal selects said selector circuit, said first and second receiver and driver pairs operate in said first operating mode.

Claim 3 (original): An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal does not select said selector circuit, said first and second receiver and driver pairs operate in said second operating mode.

Claim 4 (original): An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal selects said selector circuit, said second receiver and driver pair is deactivated to permit point-to-point data communications using said first receiver and driver pair between said I/O device and another device connected to said first data bus.

Claim 5 (original): An interface as in claim 1, wherein said first and second receiver and driver pairs are located on a same integrated circuit as a memory device.

Claim 6 (original): An interface as in claim 1, wherein said first and second receiver and driver pairs are located on a memory module.

Claim 7 (original): An interface as in claim 1, wherein said I/O device comprises a memory device.

Claim 8 (original): An interface as in claim 1, wherein said I/O device comprises a second data bus.

Claim 9 (original): A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus and receive data on said second data bus and selectively place said data on said first data bus.

Claim 10 (original): The interface of claim 9, wherein said interface circuit selects data for receipt from said first and second data buses according to a selection signal received on a command and address bus.

Claim 11 (original): The interface of claim 9, wherein said interface circuit is further configured to receive a selection signal, and said interface circuit selectively deactivates said second receiver and driver pair according to said selection signal.

Claim 12 (original): The interface of claim 11, wherein said interface circuit deactivates said second receiver and driver pair when said selection signal instructs said interface circuit to transfer data between said first and second data buses.

Claim 13 (original): The interface of claim 11, wherein said interface circuit is connected in a point-to-point data connection with another device connected to said first data bus when said second receiver and driver pair is deactivated.

Claim 14 (original): The interface of claim 11, wherein said selection signal is received on a command and address bus.

Claim 15 (original): The interface of claim 9, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

Claim 16 (original): The interface of claim 9, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

Claim 17 (original): The interface of claim 9, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

Claim 18 (original): The interface of claim 9, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 19 (original): The interface of claim 9, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 20 (original): The interface of claim 9, wherein said first bus includes a first number of data paths and said second bus includes a second number of data paths, and said first number of data paths is less than said second number of data paths.

Claim 21 (original): The interface of claim 9, wherein said second data bus is connected to at least one memory device.

Claim 22 (original): The interface of claim 9, wherein said first data bus is connected to a memory controller.

Claim 23 (original): The interface of claim 9, wherein said first data bus is connected to a processor.

Claim 24 (original): The interface of claim 9, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 25 (original): The interface of claim 9, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 26 (original): The interface of claim 9, wherein said first data bus transmits analog signals.

Claim 27 (original): The interface of claim 9, wherein said first data bus transmits digital signals.

Claim 28 (original): The interface of claim 9, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 29 (cancelled):

Claim 30 (original): The interface of claim 9, wherein said first data bus is a substantially stubless data bus.

Claim 31 (original): A memory module, comprising:

at least one memory device;

a data transfer interface connected to a first data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus.

Claim 32 (original): The memory module of claim 31, wherein said interface circuit selects data for transfer between said first and second data buses according to a selection signal received on a command and address bus.

Claim 33 (original): The memory module of claim 31, wherein said interface circuit is further configured to receive a selection signal, and said interface circuit selectively deactivates said second receiver and driver pair according to said selection signal.

Claim 34 (original): The memory module of claim 33, wherein said interface circuit deactivates said second receiver and driver pair when said selection signal instructs said interface circuit to transfer data between said first and second data buses.

Claim 35 (original): The memory module of claim 33, wherein said interface circuit is connected in a point-to-point data connection with another device connected to said first data bus when said second receiver and driver pair is deactivated.

Claim 36 (original): The memory module of claim 33, wherein said selection signal is received on a command and address bus.

Claim 37 (original): The memory module of claim 31, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

Claim 38 (original): The memory module of claim 31, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

Claim 39 (original): The memory module of claim 31, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

Claim 40 (original): The memory module of claim 31, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 41 (original): The memory module of claim 31, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 42 (original): The memory module of claim 31, wherein said first bus includes a first number of data paths and said second bus includes a second number of data paths, and said first number of data paths is less than said second number of data paths.

Claim 43 (original): The memory module of claim 31, wherein said second data bus is connected to at least one memory device.

Claim 44 (original): The memory module of claim 31, wherein said first data bus is connected to a memory controller.

Claim 45 (original): The memory module of claim 31, wherein said first data bus is connected to a processor.

Claim 46 (original): The memory module of claim 31, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 47 (original): The memory module of claim 31, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 48 (original): The memory module of claim 31, wherein said first data bus transmits analog signals.

Claim 49 (original): The memory module of claim 31, wherein said first data bus transmits digital signals.

Claim 50 (original): The memory module of claim 31, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 51 (cancelled):

Claim 52 (original): The memory module of claim 31, wherein said first data bus is a substantially stubless data bus.

Claim 53 (original): A data exchange system, comprising:

a first data bus having at least first and second bus segments;

a controller connected to place data on and receive data from said first data bus;

a processor coupled to said controller, and

a data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data on said first data bus and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus.

Claim 54 (original): A data transmission system comprising:

a processor;

a least one memory subsystem connected to said processor; and

a bus coupled to each of a controller and at least one memory subsystem interface circuit of said at least one memory subsystem, whereby said memory subsystem interface circuit couples at least one memory device to said bus, said memory subsystem interface circuit comprising a circuit for receiving data from said bus and converting it to data which can be processed by said at least one memory device and for receiving data from said at least one memory device and converting it to data which can be transmitted over said bus;

wherein said at least one memory subsystem interface circuit includes first and second receiver and driver pairs connected to respective first and second segments of said bus, said first receiver and driver pair receiving data on said first segment using said first receiver and selectively placing data on said first segment using said first driver, and said second receiver and driver pair receiving data on said second segment using said second receiver and selectively placing data on said second segment using said second driver.

Claim 55 (original): A system as in claim 54, wherein said controller resides on a same printed circuit board as said processor.

Claim 56 (original): A system as in claim 54, wherein said controller is integrated into said processor.

Claim 57 (currently amended): A method of data communication between devices in an electronic circuit, comprising:

receiving data at first and second receivers coupled to respective first and second segments of a first data bus;

driving data using first and second drivers coupled to said respective first and second segments, said driving being performed according to a selection signal, such that in a first operating mode a first receiver and driver pair passes signals between said first segment of said first data bus and an I/O device[[,]] and bypass said second segment, and in a second operating mode said first and a second receiver and driver pairs pass signals between respective adjacent bus segments and bypass said I/O device.

Claim 58 (original): A method as in claim 57, wherein said I/O device comprises a memory device.

Claim 59 (original): A method as in claim 57, wherein said I/O device comprises a second data bus.

Claim 60 (original): A method of data communication between devices in an electronic circuit, comprising:

connecting an interface circuit having first and second receiver and driver pairs to respective first and second segments of a first data bus that operates at a first data rate;

connecting said interface circuit to a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second receiver and driver pairs;

receiving and transmitting data on said second data bus;

selectively placing data received from said first bus segment on said second bus segment;

selectively placing data received from said second bus segment on said first bus segment; and

selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses.

Claim 61 (original): A method as in claim 60, wherein said selective conversion of data is performed according to a selection signal.

Claim 62 (original): A method as in claim 61, wherein said selective conversion of data is performed when said interface circuit is selected for operation by said selection signal.

Claim 63 (original): A method as in claim 61, wherein said selective conversion of data is not performed when said interface circuit is not selected for operation by said selection signal.

Claim 64 (original): A method as in claim 61, wherein said second receiver and driver pair is deactivated when said interface circuit is selected for operation by said selection signal.

Claim 65 (original): A method as in claim 61, wherein when said interface circuit is not selected for operation by said selection signal, data on said first segment of said first data bus is passed through to said second segment of said first data bus and data on said second segment is passed through to said first segment.

Claim 66 (original): A method as in claim 60, wherein said first data rate is faster than said second data rate.

Claim 67 (original): A method as in claim 60, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

Claim 68 (original): A method as in claim 60, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

Claim 69 (original): A method as in claim 60, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

Claim 70 (original): A method as in claim 69, wherein said first voltage level is less than said second voltage level.

Claim 71 (original): A method as in claim 60, wherein said first data bus connects to said first and second receiver and driver pairs using a first bus width different from a second bus width used to connect to said second data bus.

Claim 72 (original): A method as in claim 71, wherein said first bus width is less than said second bus width.

Claim 73 (original): A method as in claim 60, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

Claim 74 (original): A method as in claim 73, wherein said devices of said first technology include at least one processor.

Claim 75 (original): A method as in claim 73, wherein said devices of said second technology include at least one memory device.

Claim 76 (cancelled):

Claim 77 (original): A method as in claim 60, wherein said first data bus is a substantially stubless data bus.